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| ENGR 325 Lab 1  Building Systems with Quartus’ Qsys Tool | Abstract  This lab was focused on generating a complex system using the Altera Qsys and using the Signal Tap Logic Analyzer tool.  Daniel Ackuaku |

Below is a copy of the top level VHDL code for Lab1:

LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

USE ieee.std\_logic\_unsigned.ALL;

ENTITY Lab1 IS

PORT (

CLOCK\_50 : IN STD\_LOGIC;

GPIO\_0 : OUT STD\_LOGIC\_VECTOR (0 DOWNTO 0);

KEY : IN STD\_LOGIC\_VECTOR (0 DOWNTO 0);

UART\_RXD : IN STD\_LOGIC;

UART\_TXD : OUT STD\_LOGIC;

LCD\_DATA : INOUT STD\_LOGIC\_VECTOR (7 DOWNTO 0);

LCD\_ON : OUT STD\_LOGIC;

LCD\_BLON : OUT STD\_LOGIC;

LCD\_EN : OUT STD\_LOGIC;

LCD\_RS : OUT STD\_LOGIC;

LCD\_RW : OUT STD\_LOGIC

);

END Lab1;

ARCHITECTURE Lab1\_rtl OF Lab1 IS

component nios\_system is

port (

clk\_clk : in std\_logic := 'X'; -- clk

reset\_reset\_n : in std\_logic := 'X'; -- reset\_n

rs232\_RXD : in std\_logic := 'X'; -- RXD

rs232\_TXD : out std\_logic; -- TXD

lcd\_DATA : inout std\_logic\_vector(7 downto 0) := (others => 'X'); -- DATA

lcd\_ON : out std\_logic; -- ON

lcd\_BLON : out std\_logic; -- BLON

lcd\_EN : out std\_logic; -- EN

lcd\_RS : out std\_logic; -- RS

lcd\_RW : out std\_logic -- RW

);

end component nios\_system;

component ClockDividerCircuit is

port (

Clock : in std\_logic;

Reset\_n : in std\_logic;

ClockOut : out std\_logic

);

end component ClockDividerCircuit;

BEGIN

-- mapping the nios\_system

u0 : component nios\_system

port map (

clk\_clk => CLOCK\_50, -- clk.clk

reset\_reset\_n => KEY(0), -- reset.reset\_n

rs232\_RXD => UART\_RXD, -- rs232.RXD

rs232\_TXD => UART\_TXD, -- .TXD

lcd\_DATA => LCD\_DATA(7 DOWNTO 0), -- lcd.DATA

lcd\_ON => LCD\_ON, -- .ON

lcd\_BLON => LCD\_BLON, -- .BLON

lcd\_EN => LCD\_EN, -- .EN

lcd\_RS => LCD\_RS, -- .RS

lcd\_RW => LCD\_RW -- .RW

);

-- mapping the clock divider circuit

ClkDiv : component ClockDividerCircuit

port map (

Clock => CLOCK\_50,

Reset\_n => KEY(0),

ClockOut => GPIO\_0(0)

);

END Lab1\_rtl;

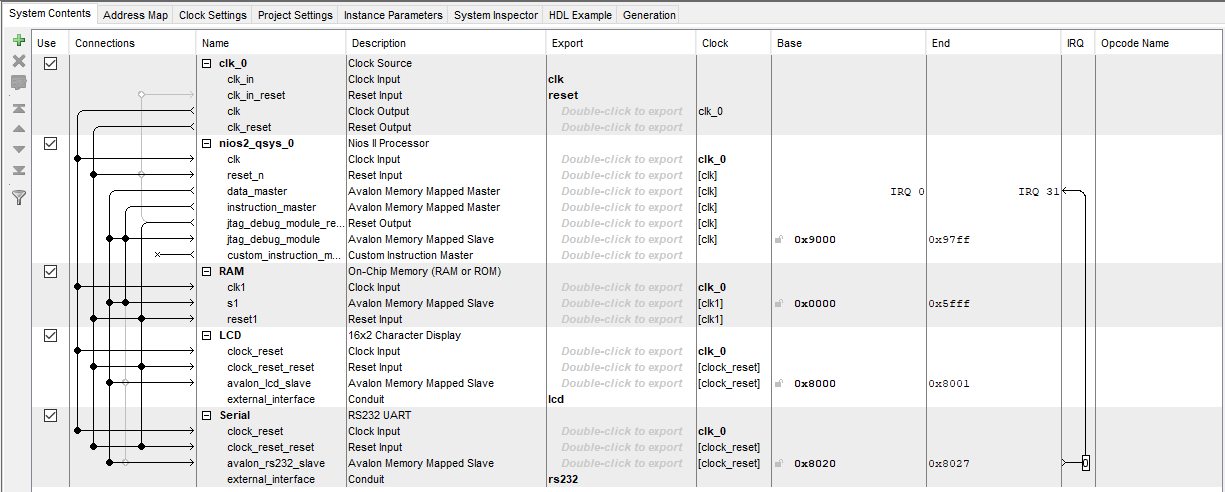
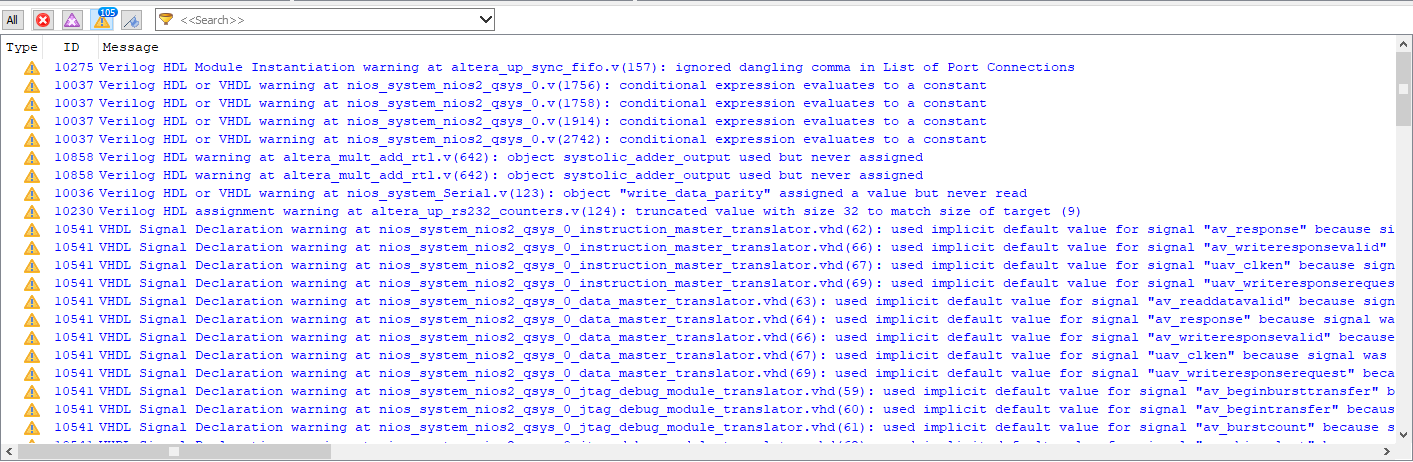
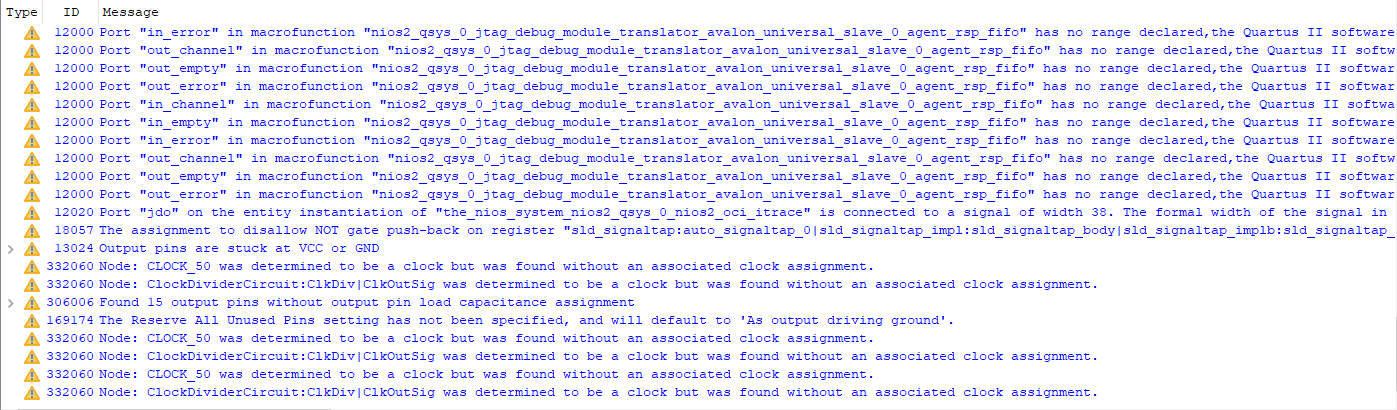


Figure 1Screen capture of the final Qsys configuration page.



Figure 2&3 Screen Capture of all Compilation warnings for the top-level design.